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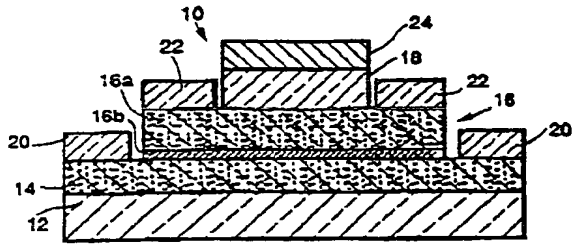
(54) NPN heterojunction bipolar transistor including antimonide base formed on semi-insulating indium phosphide substrate.

(57) A heterojunction bipolar transistor (HBT) (10, 30) includes an indium-gallium-arsenide (InGaAs), indium-phosphide (InP) or aluminum-indium-arsenide (AlInAs) collector layer (14) formed over an indium-phosphide (InP) substrate (12). A base layer (16, 32) including gallium (Ga), arsenic (As) and antimony (Sb) is formed over the collector layer (14), and an AlInAs or InP emittor layer (18) is formed over the base layer (16, 32). The base layer may be ternary gallium-arsenide-antimonide (GaAsSb) doped with beryllium (Be) (16).

FIG. 1.



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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention gonerally relates to the field of high-speed electronic transistor devices, and more specifically to an NPN heterojunction bipolar transistor (HBT) including an antimonide base formed on a semi-insulating indium phosphide (InP) substrate.

Description of the Related Art

HBTs provide substantial advantages over conventional homojunction bipolar transistors by enabling energy-gap variations in addition to electric fields as forces acting on electrons and holes. In an HBT, the emitter is designed to have a wider bandgap than the base, creating an energy barrier in the valence band at the emitter-base junction which inhibits unwanted flow of holes from the base to the emitter and substantially increases the emitter injection efficiency, current gain and operating frequency.

The wide-bandgap emitter enables very high base doping, allowing low base resistance to be obtained even with small base widths. The emitter doping can be reduced to moderate levels, allowing a reduction in base-emitter capacitance.

The advantages of HBTs have been extensively demonstrated for high-speed aluminum-gallium-arsenide/gallium-arsenide (AlGaAs/GaAs) HBTs. Moreover, alternative material systems for fabricating HBTs, including indium phosphide/indium-gallium-arsenide (InP/InGaAs) and aluminum-indium-arsenide/indium-gallium-arsenide(AlInAs/InGaAs) offer even higher performance as described in an article entitled "AlInAs/GaInAs HBT Technology", by J. Jensen et al, in IEEE Journal of Solid-State Circuits, Vol. 26, No. 3, March 1991, pp. 415-421.

However, HBTs fabricated using the latter material systems have maximum frequencies of oscillation (f_{max}) which are lower than their respective high cutoff frequencies (f_T) due to relatively high values of the product of base resistance and collector capacitance. This limits the potential speed and output power of circuits incorporating these HBTs because, as a desired design parameter, f_{max} should be approximately twice f_T.

Moreover, the base layer of InP/InGaAs and AlInAs/InGaAs/InGaAs HBTs is typically doped with beryllium (Be) as a P-type dopant. Be is highly diffusive, and migrates rapidly from the base layer into the emitter layer during growth and even during device operation, causing the P-N junction to be displaced from the emitter-base junction into the emitter layer. As a consequence, an energy barrier to electron flow is created and the barrier to hole flow is reduced, thus reducing the current gain.

Therefore, there is a need for an HBT device which overcomes these problems that has enhanced performance cnaracteristics, such as high f_{max} than the conventional HBTs, and is doped with Be or other P-type dopant without conventional notorious effects.

SUMMARY OF THE INVENTION

Accordingly, a heterojunction bipolar transistor (HBT) embodying the present invention having enhanced performance characteristics includes an indium-gallium-arsenide (InGaAs), indium-phosphide (InP) or aluminum-indium-arsenide (AlInAS) collector layer formed over an indium-phosphide (InP) semi-insulating substrate. A base layer including gallium (Ga), arsenic (As) and antimony (Sb) is formed over the collector layer, and an aluminum-indium-arsenide (AlInAs) or InP emitter layer is formed over the base layer.

The base layer may be ternary gallium-arsenide-antimonide (GaAsSb) doped with beryllium (Be), or a strained-layer-superlattice (SLS) structure including alternating superlattice layers of undoped GaAs and P-type gallium-antimonide (GaSb). The GaSb superlattice layers are preferably doped with silicon (Si), which is much less diffusive than Be and enables the HBT to be fabricated with negligible displacement of the P-N junction from the emitter-base junction into the emitter layer.

The use of Sb in the base layer rather than indium (In) and arsenic (As) as in conventional InP/InGaAs or AlInAs/InGaAs HBTs provides advantages including:

1. Higher valence band offset at the emitter-base junction, resulting in improved emitter injection efficiency.
2. Lower conduction band offset at the emitter-base junction, resulting in reduced power dissipation.
3. Reduced base resistance due, to increased hole mobility, resulting in higher f_{max}.
4. A potential barrier at the base-collector junction which reduces charge storage, also resulting in higher f_{max}.

These and other features and advantages of the present invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified fragmentary sectional view illustrating a first embodiment of an HBT embodying the present invention:

FIG. 2a is an energy band diagram illustrating a prior art HBT including an AlInAs emitter layer and an InGaAs base layer;

FIG. 2b is similar to FIG. 2a, illustrating an HBT according to the present invention including an AlInAs emitter layer and an GaAsSb base layer;

FIG. 3a is an energy band diagram illustrating a prior art HBT including an InP emitter layer and an InGaAs base layer;

FIG. 3b is similar to FIG. 3a, illustrating an HBT according to the present invention including an InP emitter layer and an GaAsSb base layer; and

FIG. 4 is a simplified fragmentary sectional view illustrating a second embodiment of an HBT embodying the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIG. 1 of the drawing, an NPN heterojunction bipolar transistor (HBT) embodying the present invention is illustrated in simplified form and generally designated as 10. The HBT 10 includes a semi-insulating InP substrate 12, an indium-gallium-arsenide ($In_{.53}Ga_{.47}As$), indium-phosphide (InP) or aluminum-indium-arsenide ($Al_{.48}In_{.52}As$) collector layer 14 which is formed over the substrate 12 and doped N-type, a ternary $Ga_yAs_{1-y}Sb$ base layer 16 which formed over the collector layer 14 and doped P-type and an InP or $Al_{.48}In_{.52}As$ emitter layer 1B which is formed over the base layer 16 and doped N-type. The value of y in the $Ga_yAs_{1-y}Sb$ base layer 16 is preferably 0.5, but is variable between 0 and 1.

The collector, base and emitter layers 14, 16 and 18 respectively are lattice matched as closely as possible to the substrate 12. Although the collector layer 14 is illustrated as being disposed between the base layer 16 and substrate 12 in the drawing, it is within the scope of the invention to reverse the relative positions of the collector layer 14 and emitter layer 18. Further illustrated are electrically conductive metal collector contacts 20, base contacts 22 and an emitter contact 24.

The HBT 10 may be fabricated using conventional technology, preferably solid-source molecular-beam-epitaxy (MBE). The fabrication process per se is not the particular subject matter of the invention.

The collector layer 14 has a thickness between approximately 250 - 500 nm, with the preferred value being 300 nm. The collector layer 14 is doped with Si to a free carrier concentration of approximately 1 - 5 x 10^{16} electrons/cm^3, with the preferred value being 1 x 10^{16}.

The emitter layer 18 has a thickness between approximately 150 - 250 nm, with the preferred value being 150 nm. The emitter layer 18 is doped with Si to a free carrier concentration at approximately 4 - 8 X 10^{17} electrons/cm^3, with the preferred value being 8 x 10^{17}.

The base layer 16 has a thickness between approximately 50 - 100 nm. In a preferred embodiment of the invention, the base layer 16 includes a 50 nm thick main layer 16a doped with Be to a free carrier concentration of approximately 3 - 6 x 10^{19} holes/cm^3, with the preferred value being 5 x 10^{19}, and a spacer layer 16b disposed between the main layer 16a and the collector layer 14. The spacer layer 16b is preferably 15 nm thick, and doped with Be to a free carrier concentration of 2 x 10^{18} holes/cm^3.

In conventional InP/InGaAs and AlInAs/InGaAs HBTs, the base layer is formed of InGaAs. However, in accordance with the present invention, the base layer 16 is formed of ternary GaAsSb doped P-type with Be. Be-doped GaAsSb in the base layer 16 provides improved performance over conventional HBTs by increasing the hole mobilities and valence band offsets to confine the holes to the base region.

FIG. 2a is an energy band diagram illustrating a prior art HBT including an AlInAs emitter layer and an InGaAs base layer, whereas FIG. 2b illustrates an HBT according to the present invention including an AlInAs emitter layer and a GaAsSb base layer. FIG. 3a is an energy band diagram illustrating a prior art HBT including an InP emitter layer and an InGaAs base layer, whereas FIG. 3b illustrates an HBT according to the present invention including an InP emitter layer and a GaAsSb base layer. The emitter, base and collector layers are designated as E, B and C respectively in the drawings.

As described in an article entitled "Band-edge alignment in heterostructures", by F. Schuermeyer et al, in Applied physics Letters, Vol. 55, No. 18, 30 Oct. 1989, pp. 1877-1878, the valence band offset ΔE_v for a GaAsSb/AlInAs heterostructure is 0.43 eV, as compared to 0.2 eV for an InGaAs/AlInAs heterostructure. The increase in ΔE_v is clearly evident from a comparison of FIGS. 2a and 2b, and provides a substantial improvement in emitter injection efficiency over the prior art by increasing the confinement of holes to the base layer 16.

As illustrated in FIGs. 3a and 3b, the increase in ΔE_v is even greater for the case of an InP emitter. The present GaAsSb base provides ΔE_v of 0.62 eV as compared to 0.33 for the conventional InGaAs base. The lattice matched emitter/base structure of InP/GaAsSb with ΔE_v = 0.62 eV pro-

vides especially efficient emitter injection efficiency.

The present invention also reduces the conduction band offset ΔE_c as compared to the prior art. This enables a reduction in base-emitter turn-on voltage V_{BE}, and a corresponding reduction in power dissipation. For the AlInAs emitter configuration illustrated in FIGs. 2a and 2b, the value of ΔE_c is reduced from the conventional value of 0.46 eV to 0.28 eV. For the InP emitter configuration illustrated in FIGs. 3a and 3b, the value of ΔE_c is reduced from the conventional value of 0.24 eV to 0.06 eV.

The present GaAsSb base 16 as lattice matched to the InP substrate 12 provides approximately twice the hole mobility than the conventional InGaAs base, resulting in reduced base resistance and higher f_{max}. More specifically, the hole mobility in GaSb is approximately 1,400 cm^2/V-sec, as compared to 430 cm^2/V-sec in InGaAs.

As further illustrated in FIGs. 2b and 3b, the present GaAsSb base configuration provides valence and conduction band offsets at the base-collector junction which are not present in the conventional InGaAs base HBTs. The valence band offset ΔE_v at the base-collector junction is 0.23 eV, whereas the corresponding conduction band offset ΔE_c is 0.18 eV. These offsets produce a potential barrier which enhances hole confinement in the base layer 16, reduces charge storage and increases f_{max}.

FIG. 4 illustrates another HBT 30 embodying the present invention, in which like reference numerals are used to designate elements which are common to the HBT illustrated in FIG. 1. The HBT 30 differs from the HBT 10 in that the ternary GaAsSb base layer 16 is replaced by a base layer 32 in the form of a strained-layer-superlattice (SLS) structure including alternating superlattice layers 32a of gallium-antimonide (GaSb) doped with Si, and undoped GaAs superlattice layers 32b.

Although the SLS base layer 32 is illustrated in simplified form as including 2.5 periods (number of pairs of superlattice layers 32a and 32b), an actual HBT 30 fabricated in accordance with the invention will include an SLS base layer 32 having approximately 21 - 27 periods with a corresponding thickness range of approximately 50 100 nm. The preferred thickness value is 65 nm, corresponding to approximately 23 periods. The SLS base layer 32 is preferably fabricated such that the resulting free carrier concentration is approximately 2 x 10^{18} holes/cm^3.

It will be understood that although Si is an N-type dopant in InGaAs, InP, AlInAs and GaAsSb, it is a P-type dopant in GaSb as described in an article entitled "p-type doping of gallium antimonide grown by molecular beam epitaxy using silicon", by T. Rossi et at, in Applied Physics Letters, Vol. 57, no. 21, 19 Nov. 1990, pp. 2256-2258. Si is much less diffusive than Be, enabling the HBT 30 to be fabricated with negligible displacement of the P-N junction from the emitter-base junction into the emitter layer 18. This also enables the fabrication process to be simplified since only one dopant material is required.

Although Be is a less preferred P-type dopant for the GaSb superlattice layers 32a, it may be used instead of Si within the scope of the invention.

The GaSb superlattice layers 32a have a compressive strain of approximately 3.5%, whereas the GaAs superlattice layers 32b have a tensile strain of approximately the same magnitude. Since the tensile and compressive strains complement each other, the SLS base layer 32 can be fabricated with an arbitrarily large number of periods if the mole fractions of Sb and As are made equal.

Increasing the mole fraction of Sb in the SLS in will improve the performance of the HBT 30 by increasing the hole mobility, reducing the conduction band offset ΔE_c and increasing the valance hand offset ΔE_v. However, the practical upper limit for increasing the Sb mole fraction is believed to be approximately 67%, above which value the SLS will become overstressed and will relax resulting in the formation of misfit dislocations. The valence band offset ΔE_v with this configuration is approximately 0.89 eV.

EXAMPLE

An HBT was fabricated as described with reference to FIG. 4, with equal mole fractions of Sb and As, and P-type doping of approximately 2 x 10^{18} holes/cm^3 in the SLS base layer 32. The average hole mobility at room temperature was approximately 800 cm^2/V-sec, four times that of a conventional HBT with an $In_{.53}Ga_{.47}As$ base doped with Be.

While several illustrative embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art, without departing from the spirit and scope of the invention. Accordingly, it is intended that the present invention not be limited solely to the specifically described illustrative embodiments. Various modifications are contemplated and can be made without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. An NPN type heterojunction bipolar transistor (HBT), characterized by:

- an emitter layer (18) including a material selected from the group consisting of aluminum-indium-arsenide (AlInAs) and indium phosphide (InP);
- a base layer (16; 32) including gallium (Ga), arsenic (As) and antimony (Sb); and
- a collector layer (14).

2. The transistor of claim 1, characterized by a substrate (12), said emitter, base and collector layers (18, 16, 14) being formed over said substrate (12).

3. The transistor of claims 1 or 2, characterized in that said base layer (16; 32) is disposed between said emitter and collector layers (18, 14).

4. The transitor of any of claims 1 through 3, characterized in that said emitter layer (18) is doped N-type.

5. The transistor of any of claims 1 through 4, characterized in that said base layer (16; 32) is doped P-type.

6. The transistor of any of claims 1 through 5, characterized in that said collector layer (14) comprises a material selected from the group consisting of indium-gallium-arsenide (InGaAs), indium-phosphide (InP) and aluminum-indium-arsenide (AlInAs).

7. The transistor of claim 6, characterized in that said collector layer (14) is doped N-type.

8. The transistor of any of claims 2 through 7, characterized in that said substrate (12) comprises indium-phosphide (InP).

9. The transistor of any of claims 2 through 8, characterized in that said substrate (12) is semi-insulating.

10. The transistor of any of claims 1 through 9, characterized in that said collector layer (14) is disposed between said substrate (12) and said base layer (16; 32).

11. The transistor of any of claims 1 through 10, characterized in that said base layer (16; 32) comprises gallium-arsenide-antimonide (GaAsSb), preferably ternary gallium-arsenide-antimonide (GaAsSb).

12. The transistor of any of claims 1 through 11, characterized in that said base layer (16; 32) is doped with beryllium (Be).

13. The transistor of any of claims 1 through 12, characterized in that said base layer (32) comprises a strained-layer-superlattice (SLS) structure including alternating superlattice layers (32a, 32b) of gallium-arsenide (GaAs) and gallium-antimonide (GaSb).

14. The transistor of claim 13, characterized in that said gallium-antimonide (GaSb) superlattice layer (32a) is P-doped.

15. The transistor of claim 13, characterized in that said gallium-arsenide (GaAs) superlattice layer (32b) is P-doped.

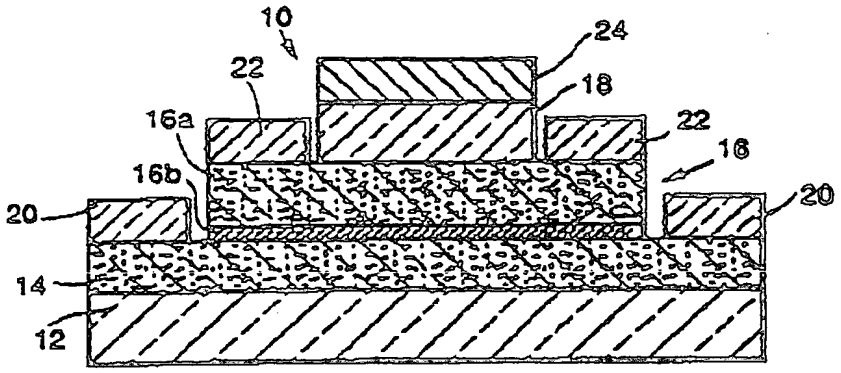
16. The transistor of any of claims 13 to 15, characterized in that said gallium-antimonide GaSb superlattice layers (32a) are doped with silicon (Si).

17. The transistor of any of claims 13 to 15, characterized in that said GaAs superlattice layers (32b) are doped with beryllium (Be).

18. The transistor of any of claims 13 to 15, characterized in that said superlattice layers (32a, 32b) are undoped.

19. The transistor of any of claims 13 to 18, characterized in that said superlattice structure has 21 - 27 periods.

FIG. 1.



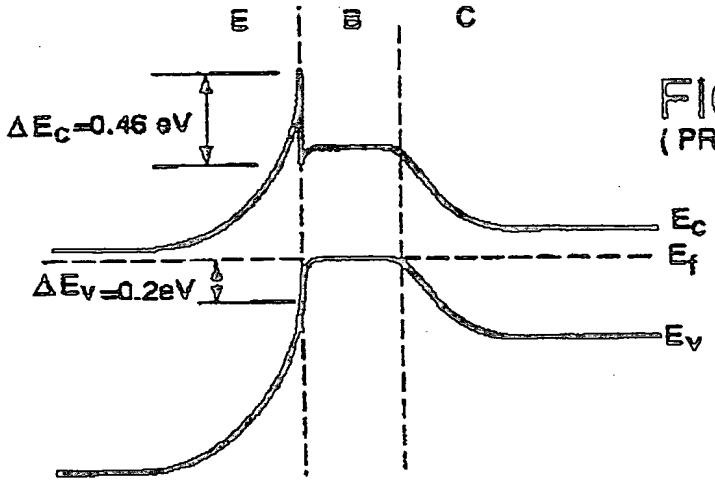


FIG. 2a.
(PRIOR ART)

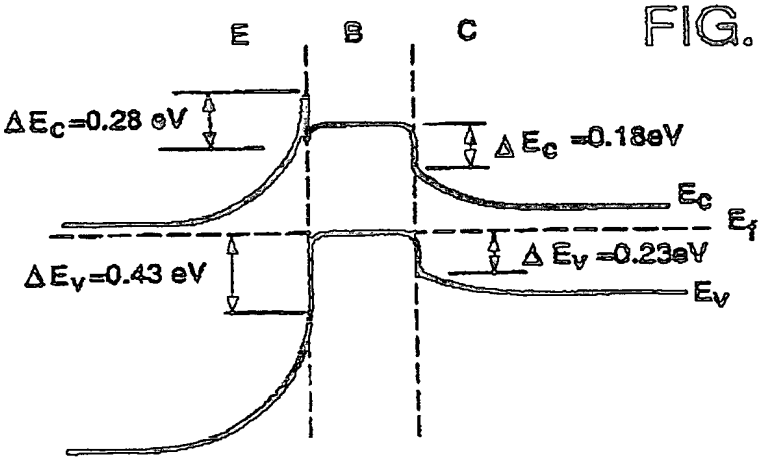


FIG. 2b.

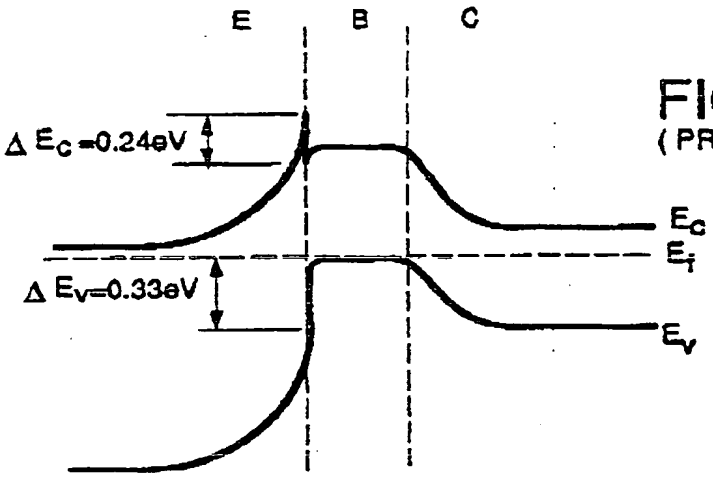


FIG. 3a.
(PRIOR ART)

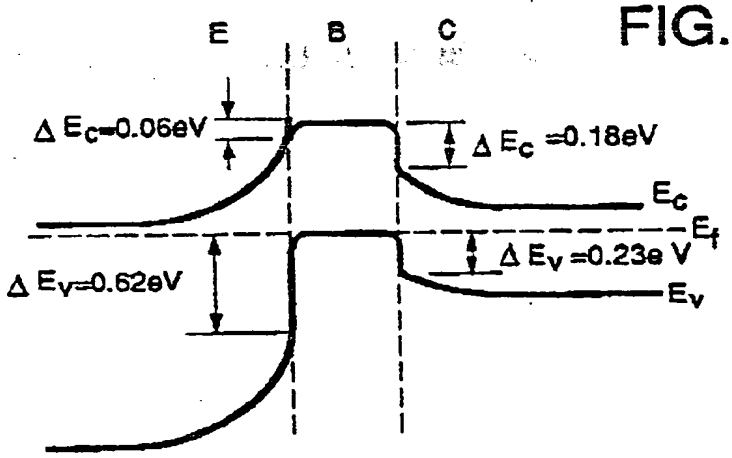


FIG. 3b.

FIG. 4.

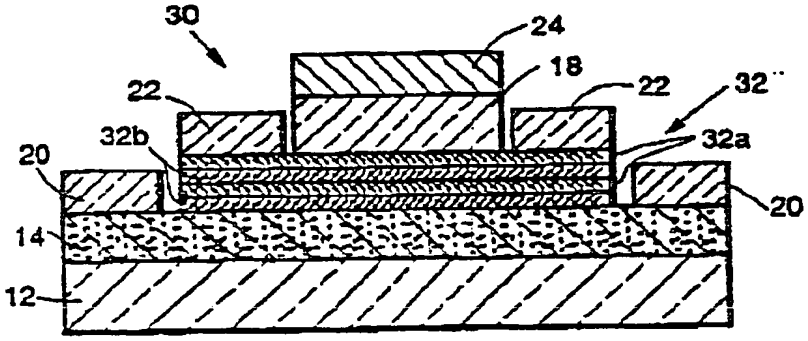


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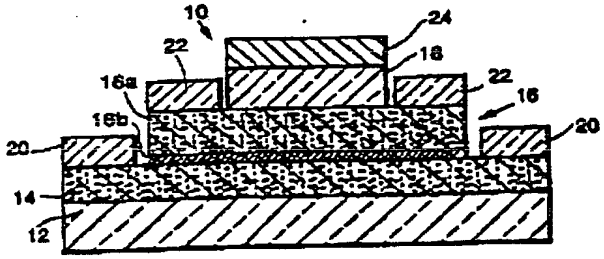
FIG. 1.



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EUROPEAN SEARCH REPORT

Application Number
EP 93 10 8534

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 385 (E-1249) 17 August 1992 & JP-A-04 124 830 (FUJITSU LTD) 24 April 1992 * abstract *	1-8,10, 11	H01L29/73 H01L29/205 H01L29/14
Y	* abstract * ---	13	
Y	EP-A-0 133 342 (NIPPON ELECTRIC CO) 20 February 1985 * claims * ---	13	
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 302 (E-0946) 28 June 1990 & JP-A-02 097 026 (FUJITSU LTD) 9 April 1990 * abstract * ---	1-8,10, 11	
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 170 (E-1062) 30 April 1991 & JP-A-03 038 835 (NEC CORP) 19 February 1991 * abstract * ---	1-8,10, 11	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A	ELECTRONICS LETTERS, 5 JULY 1990, UK, VOL. 26, NR. 14, PAGE(S) 965 - 967, ISSN 0013-5194 Khamsehpour B et al 'GaAs-GaAsSb based heterojunction bipolar transistor' -----	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 May 1994	Lina, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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